Aeonic Generate™ AWM

High Performance SoC Advanced Clock Generation Module

DATA SHEET

The Movellus™ Aeonic Generate Adaptive Workload Module (AWM) family of high-performance clock generation IP products are part of the Aeonic Intelligent Clock Network™ architecture. Designed for high reliability and fully SCAN enabled, the AWM provides extensive visibility and controllability of key clocking metrics.

Movellus AWMs have the optimal Power, Performance, and Area (PPA) characteristics needed for high-performance, power-efficient SoC clocking applications. The Aeonic Generate AWM family supports glitchless frequency changes for Dynamic Voltage and Frequency Scaling (DVFS) applications and rapidly change frequencies for droop response, resulting in more reliable performance with dynamic workloads and power efficiency. The AWM clock generator provides eight unique clock outputs in the smallest area possible.

The Movellus Aeonic Generate product family is intrinsically flexible because it is built with synthesizable Verilog. Movellus' expertise lies in converting traditionally analog functions to digital and this has allowed the company to develop feature-rich digital IP that is synthesizable. With proven process portability (65 nm to 3 nm) and minimal area footprint, the AWM is ideally suited for large scale distribution within an SoC.

Features

- Process portable
- Proven (65nm to 3nm)
- Core voltage supply
- Low jitter
- Low power
- Detailed debug hooks
- Multi-instance
- Ultra-low voltage
- Fine grain frequency control

Applications

- AI processors
- CPU
- GPU
- Memory pooling
- Aerospace
- Automotive

Foundries

- TSMC
- Intel
- Global Foundries
- UMC
- Fujitsu

Product Specifications

Parameter	Value
Input Frequency	38 kHz – 200 MHz
Input Clocks	1
Output Frequency	See Process Table
Output Clocks	8
Period Jitter (P-P)	±1.5%
Duty Cycle	48 - 52%
Frequency Transition Time	5 high-speed cycles
Frequencies for Fast Switch	2 - 8
Frequency Lock Time	130 REFCLK cycles
Area	See Process Table
Power	See Process Table
APB Frequency	100 MHz
JTAG Frequency	100 MHz
SCAN Frequency	50 MHz

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AWM High-Level Block Diagram

Figure 1 below shows a block diagram of the Aeonic AWM Clock Generation Module.

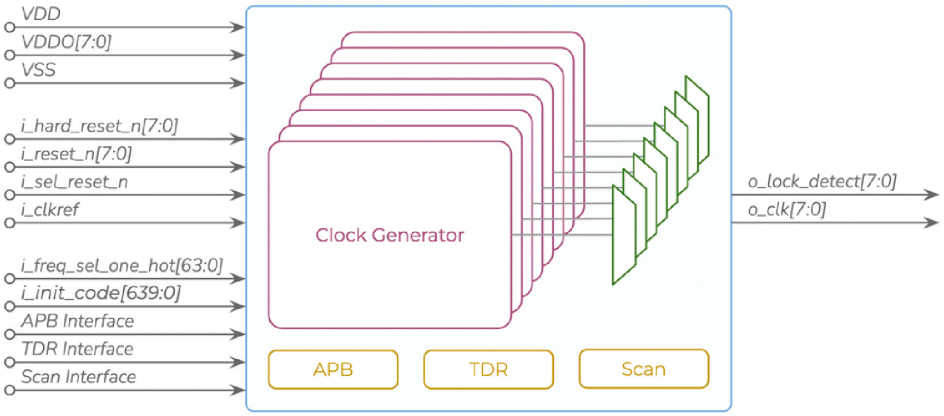

Figure 1. AWM Block Diagram

The block diagram contains the logic blocks described below.

Interfaces

The AWM contains the three interface types as shown at the bottom of Figure 1.

- APB: The APB interface supports the standard AMBA APB interface, which is used to program internal registers for the Aeonic Generate AWM.
- TDR: The TDR interface is an IEEE 1149.1 JTAG-compliant interface for testing and debugging the AWM, and it is controlled through a JTAG TAP controller.
- SCAN: The Scan interface supports an input scan clock and signal and allows external chain stitching.

Functional Blocks

Each of the eight clock generator blocks shown in Figure 1 contains the following elements.

- Pre-divider: These eight dividers set the pre-division ratio for input into each fractional clock generator.
- Fractional Clock Gen: Each clock generator has a fractional or integer multiple (14 bits) of the input clock signal from the pre-divider for each of the eight output clocks.
- Post-divider: Each AWM has eight post-dividers (corresponding to the width of o_clk[7:0]), one for each output clock. The block supports integer division of the fractional clock gen output.
- Controller: The controller takes the input signals into the AWM and sets the sub-block registers.

General Pin Descriptions

Pin Name	I/O	Description
i_hard_reset_n[7:0]	I	Hard Reset. The AWM contains eight hard reset pins, one per clock generator. Each hard reset signal is active LOW. Although this signal serves as a master reset for both the core logic and the APB interface, the TDR is unaffected by this signal. This reset is asserted asynchronously and deasserted synchronously using the respective clock domain.
i_reset_n[7:0]	I	Core Reset. The AWM contains eight reset pins, one per clock generator. Each core reset is active LOW and resets the core registers. This reset signal is asserted asynchronous and deas-serted synchronously using the reference clock.
i_sel_reset_n	I	Frequency selection reset.
i_refclk	I	Reference Clock. The low frequency reference clock for the system.
i_freq_sel_one_hot[63:0]	I	o_clk[7:0] frequency selection.

Pin Name	I/O	Description
o_clk[7:0]	O	Output Clock. Eight high frequency output clocks generated by the system.
o_lock_detect[7:0]	O	Lock Detect. Indicates that the feedback loop within the system has stabilized, and the output clocks are operating as expected. There are eight lock detect output signals, one per clock generator.
i_init_code[639:0]	I	Defines the initial state for each of the clock generator cores.

APB Interface Pin Descriptions

Pin Name	I/O	Description
i_preset_n	I	Reset. The APB reset signal is active LOW. This signal can be connected directly to the system bus reset signal.
i_pclk	I	Clock. All transfers timed on the rising edge.
i_paddr[9:0]	I	Address. This is the APB address bus and is driven by the peripheral bus bridge unit.
i_psel	I	Select. Indicates the device is selected and that a data transfer is required.
i_penable	I	Enable. This signal indicates the second and subsequent cycles of an APB transfer.
i_pwrite	I	Direction. This signal indicates an APB write access when HIGH and an APB read access when LOW.
i_pwdata[15:0]	I	Write Data. Data to write to i_paddr address when a write command is requested.
i_pstrb[1:0]	I	Write Strobes. This signal indicates which byte lanes to update during a write transfer. There is one write strobe for each eight bits of the write data bus. Write strobes must not be active during a read transfer.
o_prdata[15:0]	O	Read Data. Data read from i_paddr address after a successful read command is requested.
o_pready	O	Ready. This signal is used to extend an APB transfer.
o_pslverr	O	Slave Error. This signal indicates a transfer failure when HIGH.

JTAG Pin Descriptions

Pin Name	I/O	Description
i_tdr_readback	I	Readback. The TDR feedback signal is active HIGH and provides a mechanism to read back the internal TDR register values. When active, a TDR capture moves the internal register values into the shift chain for readout. When low, a TDR capture samples the state of the IP pins. For writable registers, readback capture samples the register output. For read-only registers, readback capture samples the value of the current internal shift state.
i_tdr_mode	I	Mode. The TDR mode signal is active HIGH and enables the TDR to directly control the pins of the IP.
i_tdr_clk	I	Clock. All transfers are sampled on the rising edge and updated on the falling edge.
i_tdr_rst_n	I	Reset. The TDR reset signal is active LOW. This signal can be connected directly to the top-level TAP reset.
i_tdr_select[8:0]	I	Select. This signal is active HIGH and indicates that the TDR is active. The TDR will only capture, shift, and update when active.
i_tdr_capture	I	Capture. This signal is active HIGH and executes a capture operation.
i_tdr_shift	I	Shift. This signal is active HIGH and executes a shift operation.
i_tdr_update	I	Update. This signal is active HIGH and executes an update operation.
i_tdr	I	Input. Data to shift into the TDR shift registers.
o_tdr	O	Output. Data shifted out of the TDR shift registers.

SCAN Interface Pin Descriptions

Pin Name	I/O	Description
i_scan_clk	I	Clock. The scan clock is the clock signal used during scan test mode. This clock is used for shifting, launch, and capture while scan mode is active.

Pin Name	I/O	Description
i_scan_en	I	Enable. The scan enable signal is active HIGH and enables shifting between the scan inputs and scan outputs through the scan cells.
i_scan_mode	I	Mode. The scan mode signal is active HIGH and activates the test mode.
i_scan[66:0]	I	Input. Data to shift into the scan chains.
o_scan[66:0]	O	Output. Data shifted out of the scan chains.

Example Process Implementations

Process	Output Frequency	Feedback Division	Area [1] (8F Version)	Supply Voltage	Power[1]
22 nm	78 MHz - 2.5 GHz	14b fractional	503 μm x 503 μm	0.72V - 0.88V	76 mW @ 2 GHz
12 nm	56 MHz - 3.5 GHz	14b fractional	375 μm x 375 μm	0.72V - 0.88V	52 mW @ 3.5 GHz
12 nm (rad-hard)	33 MHz - 1 GHz	14b fractional	645 μm x 645 μm	0.72V - 0.88V	82 mW @ 1 GHz
7 nm	2 MHz - 4 GHz	14b fractional	207 μm x 207 μm	0.59V - 0.93V	78 mW @ 4 GHz
5 nm	65 MHz - 4 GHz	14b fractional	182 μm x 182 μm	0.59V - 0.83V	65 mW @ 4 GHz
3 nm	65 MHz - 5 GHz	14b fractional	160 μm x 160 μm	0.55V - 0.95V	47 mW @ 5 GHz

1. Actual power and area are implementation specific and will vary based on factors such as process node, standard cell library, operating temperature, operating voltages, and process variations.

Deliverables

The Aeonic AWM is delivered as encrypted Verilog, with corresponding test-benches, for simulation and integration. The delivered package also has an IPXACT file for register mapping and a placement map for floor-planning. Movellus provides the appropriate constraint files for synthesis, place and route, and timing analysis. Additionally, a gate-level netlist is provided for DFT integration and verification.

Movellus Aeonic Product Line

Product	Description
Aeonic Generate™ CGM	High performance SoC clock generation module with multiple outputs.
Aeonic Generate™ AWM	Advanced function clock generation module with multiple independent outputs.
Aeonic Connect™	Intelligent Clock Network™ platform for clock distribution in complex monolithic ICs and chiplet based architectures.

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