MOVELLUS™

Aeonic Generate™ CGM

High Performance SoC Clock Generation Module

DATA SHEET

The Movellus™ high-performance Aeonic Generate Clock Generation Module (CGM) is a high-quality clock synthesis IP that is part of the Movellus Aeonic™ platform.

The Movellus Aeonic Generate product family is intrinsically flexible because it is built with synthesizable Verilog. Movellus' expertise lies in converting traditionally analog functions to digital and this has allowed the company to develop feature-rich digital IP that is synthesizable. The product is delivered as soft IP and implemented using the customer's standard cell library. With proven process portability (65 nm to 3 nm) and minimal area footprint, the CGM is ideally suited for large scale distribution within an SoC.

Features

- Process portable
- Proven (65nm to 3nm)
- Core voltage supply
- Low jitter
- Low power
- Detailed debug hooks
- Multi-instance
- Ultra-low voltage
- Fine grain frequency control

Applications

- AI processors
- CPU
- GPU
- Vision processing
- Crypto mining
- Memory pooling
- Satellite
- Edge AI
- Voice recognition
- Aerospace
- Automotive

Foundries

- TSMC
- Intel
- Global Foundries
- UMC
- Fujitsu

Product Specifications

Parameter	Value
Input Frequency	38 kHz – 200 MHz
Input Clocks	1
Output Frequency	See Process Table
Output Clocks	8
Period Jitter (P-P)	±1.5%
Duty Cycle	48 - 52%
Frequency Lock	130 REFCLK cycles
Area	See Process Table
Power	See Process Table
APB Frequency	100 MHz
JTAG Frequency	100 MHz
SCAN Frequency	50 MHz

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CGM High-Level Block Diagram

Figure 1 below shows a block diagram of the Aeonic Clock Generation Module (GCM).

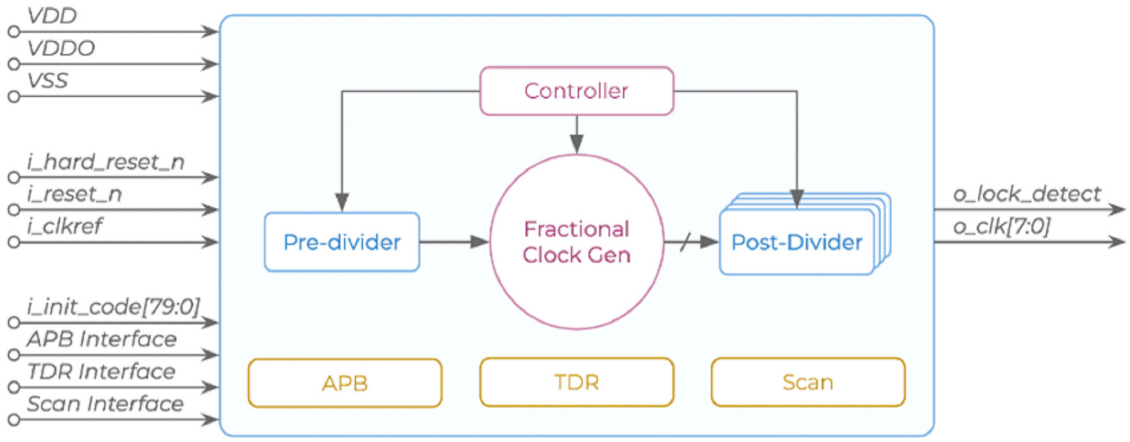

Figure 1. CGM Block Diagram

The block diagram contains the logic blocks described below.

Interfaces

The CGM contains the three interface types shown at the bottom of Figure 1.

- APB: The APB interface supports the standard AMBA APB interface, which is used to program internal registers for the Aeonic Generate CGM.
- TDR: The TDR interface is an IEEE 1149.1 JTAG compliant interface for testing and debugging the CGM. It is controlled through a JTAG TAP controller.
- Scan: The Scan interface supports an input scan clock and signal and allows external chain stitching.

Functional Blocks

The CGM contains the functional blocks shown in Figure 1.

- Pre-divider: Sets the pre-division ratio for input into the fractional clock generator.
- Fractional Clock Gen: The fractional clock generation block can output a fractional or integer multiple (14 bits) of the input clock signal from the pre-divider.
- Post-divider: Each CGM can have up to eight post-dividers (corresponding to the width of o_clk). The block supports integer division of the fractional clock gen output.
- Controller: The controller takes the input signals into the CGM and sets the sub-block registers.

General Pin Descriptions

Pin Name	I/O	Description
i_hard_reset_n	I	Hard Reset. The hard reset signal is active LOW. Although this signal serves as a master reset for both the core logic and the APB interface, the TDR is unaffected by this signal. This reset is asserted asynchronously and deasserted synchronously using the respective clock domain.
i_reset_n	I	Core Reset. The core reset is active LOW and resets the core registers. This reset signal is asserted asynchronous and deasserted synchronously using the reference clock.
i_refclk	I	Reference Clock. The low frequency reference clock for the system.
o_clk[7:0]	O	Output Clock. High frequency output clocks generated by the system.
o_lock_detect	O	Lock Detect. Indicates that the feedback loop within the system has stabilized, and the output clocks are operating as expected.

Pin Name	I/O	Description
i_init_code[79:0]	O	Initialization Code. The initialization code is a configurable interface that defines the state of the system after reset. This signal is typically used to define the startup behavior coming out of reset.

APB Interface Pin Descriptions

Pin Name	I/O	Description
i_pclk	I	Clock. All transfers timed on the rising edge.
i_preset_n	I	Reset. The APB reset signal is active LOW. This signal can be connected directly to the system bus reset signal.
i_paddr[4:0]	I	Address. This is the APB address bus and is driven by the peripheral bus bridge unit.
i_psel	I	Select. Indicates the device is selected and that a data transfer is required.
i_penable	I	Enable. This signal indicates the second and subsequent cycles of an APB transfer.
i_pwrite	I	Direction. This signal indicates an APB write access when HIGH and an APB read access when LOW.
i_pwdata[15:0]	I	Write data. Data to write to i_paddr address when a write command is requested.
i_pstrb[1:0]	I	Write Strobes. This signal indicates which byte lanes to update during a write transfer. There is one write strobe for each eight bits of the write data bus. Write strobes must not be active during a read transfer.
o_pready	O	Ready. This signal is used to extend an APB transfer.
o_prdata[15:0]	O	Read Data. Data read from i_paddr address after a successful read command is requested.
o_pslverr	O	This signal indicates a transfer failure when HIGH.

JTAG Pin Descriptions

Pin Name	I/O	Description
i_tdr_mode	I	Mode. The TDR mode signal is active HIGH and enables the TDR to directly control the pins of the IP.
i_tdr_clk	I	Clock. All transfers are sampled on the rising edge and updated on the falling edge.
i_tdr_rst_n	I	Reset. The TDR reset signal is active LOW. This signal can be connected directly to the top-level TAP reset.
i_tdr_select	I	Select. This signal is active HIGH and indicates that the TDR is active. The TDR will only capture, shift, and update when active.
i_tdr_capture	I	Capture. This signal is active HIGH and executes a capture operation.
i_tdr_shift	I	Shift. This signal is active HIGH and executes a shift operation.
i_tdr_update	I	Update. This signal is active HIGH and executes an update operation.
i_tdr_readback	I	Readback. The TDR feedback signal is active HIGH and provides a mechanism to read back the internal TDR register values. When active, a TDR capture moves the internal register values into the shift chain for readout. When low, a TDR capture samples the state of the IP pins. For writable registers, readback capture samples the register output. For read-only registers, readback capture samples the value of the current internal shift state.
i_tdr	I	Input. Data to shift into the TDR shift registers.
o_tdr	O	Output. Data shifted out of the TDR shift registers.

SCAN Interface Pin Descriptions

Pin Name	I/O	Description
i_scan_mode	I	Mode. The scan mode signal is active HIGH and activates the test mode.
i_scan_clk	I	Clock. The scan clock is the clock signal used during scan test mode. This clock is used for shifting, launch, and capture while scan mode is active.
i_scan_en	I	Enable. The scan enable signal is active HIGH and enables shifting between the scan inputs and scan outputs through the scan cells.
i_scan[6:0]	I	Input. Data to shift into the scan chains.

Pin Name	I/O	Description
o_scan[6:0]	O	Output. Data shifted out of the scan chains.

Example Process Implementations

Process	Output Frequency	Feedback Division	Supply Voltage	Area [1]	Power[1]
28 nm	56 MHz - 3.5 GHz	14b fractional	0.81V - 0.99V	220 µm x 220 µm	14 mW @ 3.5 GHz
	1 MHz - 200 MHz	14b fractional	0.81V - 0.99V	225 µm x 225 µm	80 µW @ 100 MHz
22 nm (rad-hard)	16 MHz - 1 GHz	14b fractional	0.72V - 0.88V	169 µm x 169 µm	21 mW @ 1 GHz
12 nm	56 MHz - 3.5 GHz	14b fractional	0.72V - 0.88V	91 µm x 91 µm	7 mW @ 1.8 GHz
12 nm (rad-hard)	33 MHz - 1 GHz	14b fractional	0.72V - 0.88V	202 µm x 202 µm	14 mW @ 1 GHz
7 nm	2 MHz - 4 GHz	14b fractional	0.59V - 0.93V	65 µm x 65 µm	10 mW @ 4 GHz
5 nm	65 MHz - 4 GHz	14b fractional	0.59V - 0.83V	55 µm x 55 µm	8 mW @ 4 GHz
3 nm	65 MHz - 5 GHz	14b fractional	0.55V - 0.95V	50 µm x 50 µm	6 mW @ 5 GHz

1. Actual power and area are implementation specific and will vary based on factors such as process node, standard cell library, operating temperature, operating voltages, and process variations.

Deliverables

The Aeonic CGM is delivered as encrypted Verilog, with corresponding test-benches, for simulation and integration. The delivered package also has an IPXACT file for register mapping and a placement map for floor-planning. Movellus provides the appropriate constraint files for synthesis, place and route, and timing analysis. Additionally, a gate-level netlist is provided for DFT integration and verification.

Movellus Aeonic Product Line

The table below provides general information about the Movellus product line. For more information, contact your sales representative or send an inquiry to sales@movellus.com

Product	Description
Aeonic Generate™ CGM	High performance SoC clock generation module with multiple outputs.
Aeonic Generate™ AWM	Advanced function clock generation module with multiple independent outputs.
Aeonic Connect™	Intelligent Clock Network™ platform for clock distribution in complex monolithic ICs and chiplet based architectures.